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10/077,947	02/20/2002	Hideki Okuyama	8039-1001	3041

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YOUNG & THOMPSON
745 SOUTH 23RD STREET 2ND FLOOR
ARLINGTON, VA 22202

EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/077,947	Applicant(s) OKUYAMA, HIDEKI	
	Examiner Trisha U. Vu	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 are presented for examination.

Claim Objections

2. Claim 18 is objected to because of the following informalities: "firs" (line 7) should be changed to "first". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 8-10, 12-14, and 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kregness et al. (4,984,153) (hereinafter Kregness).

As to claim 1, Kregness teaches a multiprocessor system comprising: a plurality of processors (PROC A, PROC B,...) which send and receive predetermined information to and from each other; and a shared memory (shared memory 18) which is shared and accessed by said plurality of processors one after another (Fig. 1), and wherein each of said plurality of processors requests at least one of other processors included in said plurality of processors to access said shared memory that is to be done by the at least one of other processors, in a case where each of said plurality of processors has accessed said

shared memory (e.g. releasing control to another processor to perform its test) (col. 4, lines 29-61).

As to claim 2, Kregness further teaches each of said plurality of processors requests, in a case where each of said plurality of processors has normally updated predetermined data in said shared memory (if the test is successful), the at least one of other processors to read same data as the predetermined data from said shared memory (col. 4, lines 53-61).

As to claim 3, Kregness further teaches each of said plurality of processors requests, in a case where each of said plurality of processors has not normally updated predetermined data in said shared memory (if the test is unsuccessful), the at least one of other processors to update the predetermined data in said shared memory (col. 4, lines 53-61).

As to claim 4, Kregness teaches a multiprocessor system comprising: a plurality of processors (PROC A, PROC B,...) which send and receive predetermined information to and from each other; a shared memory (shared memory 18) which is shared and accessed by each of said plurality of processors, and an access manager (arbitration logic) which manages access to said shared memory by each of said plurality of processors (col. 3, lines 61-68), and wherein said access manager selects, in a case where said plurality of processors are in contention to access said shared memory, one of said plurality of processors being in contention and permits the selected processor to access said shared memory (col. 4, lines 13-28), and each of said plurality of processors requests at least one of other processors included in said plurality of processors to access said shard memory

that is to be done by the at least one of other processors, in a case where each of the processors is selected by said access manager and the selected processor accesses said shared memory (e.g. releasing control to another processor to perform its test) (Fig. 1 and col. 4, lines 29-61).

As to claim 8, Kregness teaches a multiprocessor system comprising: a plurality of processors (PROC A, PROC B,...) which send and receive a predetermined signal to and from each other; a shared memory (shared memory 18) which is shared and accessed by each of said plurality of processors; and a contention determiner (arbitration logic) which detects whether said plurality of processors are in contention to access said shared memory, and permits one of said plurality of processors to access said shared memory (col. 3, lines 61-68), and wherein each of said plurality of processors outputs a access-request signal to at least one of other processors included in said plurality of processors, so as to request the at least one of other processors to access said shared memory, in a case where each of said plurality of processor is permitted to access said shared memory by said contention determiner and the permitted processor accesses said shared memory (e.g. releasing control to another processor to perform its test) (Fig. 1 and col. 4, lines 29-61).

As to claim 12, Kregness teaches a shared-memory controlling method to be executed in a multiprocessor system including a plurality of processors (PROC A, PROC B,...) which send and receive predetermined information to and from each other, a shared memory (shared memory 18) which is shared and accessed by each of said plurality of processors, and an access manager (arbitration logic) which manages access to said

shared memory by each of said plurality of processors, and said method comprising: selecting one processor included in said plurality of processors, and permitting the selected one processor to access said shared memory, in a case where said plurality of processors are in contention for said shared memory (col. 3, lines 61-68 and col. 4, lines 13-28); performing first access to said shared memory using the selected processor, requesting at least one of other processors included in said plurality of processors to perform second access to said shared memory, in a case where said performing the first access to said shared memory has been done; and performing the second access to said shared memory using the at least one of other processors (e.g. releasing control to another processor to perform its test) (Fig. 1 and col. 4, lines 29-61).

As to claims 5, 9, and 13, Kregness further teaches each of said plurality of processors requests, in a case where each of said plurality of processors has normally updated predetermined data in said shared memory (if the test is successful), the at least one of other processors to read same data as the predetermined data from said shared memory (col. 4, lines 53-61).

As to claims 6, 10, and 14, Kregness further teaches each of said plurality of processors requests, in a case where each of said plurality of processors has not normally updated predetermined data in said shared memory (if the test is unsuccessful), the at least one of other processors to update the predetermined data in said shared memory (col. 4, lines 53-61).

As to claim 16, Kregness teaches a shared-memory controlling method comprising: selecting one of a plurality of processors (PROC A, PROC B,...), and

permitting the selected processor to access a shared memory (shared memory 18) shared by the plurality of processors, in a case where the plurality of processors are in contention for the shared memory (Fig. 1 and col. 3, lines 61-68); performing first access to said shared memory using the selected processor; requesting at least one of other processors included in said plurality of processors to perform second access to said shared memory, in a case where the first access has been done; and performing the second access to said shared memory using the at least one of other processors (e.g. releasing control to another processor to perform its test) (Fig. 1 and col. 4, lines 29-61).

As to claim 17, Kregness teaches a computer readable recording medium for controlling a computer to execute a shared-memory controlling method comprising: selecting one processor included in a plurality of processors (PROC A, PROC B,...), and permitting the selected one processor to access a shared memory (shared memory 18), in a case where said plurality of processors are in contention for said shared memory (Fig. 1 and col. 3, lines 61-68); performing first access to said shared memory using the selected processor; requesting at least one of other processors included in said plurality of processors to perform second access to said shared memory, in a case where said performing the first access to said shared memory has been done; and performing the second access to said shared memory using the at least one of other processors (e.g. releasing control to another processor to perform its test) (Fig. 1 and col. 4, lines 29-61).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7, 11, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kregness et al. (4,984,153) (hereinafter Kregness) in view of Hauck et al. (6,587,904) (hereinafter Hauck).

As to claims 7, 11, and 15, the argument above for claims 4, 11, and 12 apply. However, Kregness does not explicitly disclose each of said plurality of processors requests, in a case where a predetermined period of time has elapsed without being selected by said access manager, the at least one of other processors and said access manager to perform a predetermined reset operation for resetting themselves. Hauck teaches detecting if arbitration is not won within a specified amount of time and requesting a long bus reset (at least col. 8, lines 56-67 and col. 12, lines 8-16). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include detecting if arbitration is not won within a specified amount of time and requesting a long bus reset as taught by Hauck by each of the plurality of processors in the system of Kregness to allow reconfiguration of the bus and connected devices to better provide the actual status of the system.

5. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kregness et al. (4,984,153) (hereinafter Kregness) in view of Mogul (6,704,798).

As to claim 18, Kregness teaches a method for controlling a computer to execute a shared-memory comprising: selecting one of a plurality of processors (PROC A, PROC B,...), and permitting the selected processor to access a shared memory (shared memory 18) shared by the plurality of processors, in a case where the plurality of processors are in contention for the shared memory (Fig. 1 and col. 3, lines 61-68); performing first access to said shared memory using the selected processor; requesting at least one of other processors included in said plurality of processors to perform second access to said shared memory, in a case where the first access has been done; and performing the second access to said shared memory using the at least one of other processors (e.g. releasing control to another processor to perform its test) (Fig. 1 and col. 4, lines 29-61). However, Kregness does not explicitly disclose the method is contained within a data signal embedded in a carrier wave representing an instruction sequence. Mogul teaches implementing a data signal embedded in a carrier wave representing an instruction sequence (col. 14, lines 4-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method via a data signal embedded in a carrier wave representing an instruction sequence as taught by Mogul in the system of Kregness to allow the method to be stored and executed in a distributed fashion over the network.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses shared memory system:

US Patent	5,813,016	Sumimoto
US Patent	5,884,046	Antonov
US Patent	5,978,839	Okuhara et al.
US Patent	5,339,427	Elko et al.
US Patent	5,418,913	Fujimoto
US Patent	6,715,059	Miller
US Patent	6,173,375	Arshad

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu

Trisha U. Vu
Examiner
Art Unit 2112

uv

Sumati Lefkowitz

SUMATI LEFKOWITZ
PRIMARY EXAMINER